Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 11 (Canceled):

12 (currently amended): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, ~~active surface regions having been defined in the surface of the substrate~~liner oxides with exposed surfaces formed over said substrate and on sidewalls of said gate electrode, gate spacers formed on said liner oxides;

~~creating a layer of gate oxide over the surface of the substrate;~~

~~depositing a layer of gate material over the surface of the substrate;~~

~~patterning and etching the layer of gate material and the layer of gate oxide, creating a gate electrode structure;~~

~~creating a layer of liner oxide over the surface of said substrate, including sidewalls and the surface of said gate electrode;~~

~~depositing a layer of gate spacer material over the surface of said layer of liner oxide;~~

~~etching said layer of gate spacer material, creating gate spacers over sidewalls of said gate electrode, thereby removing said layer of liner oxide from the surface of from sidewalls of said gate electrode where said layer of liner oxide is not covered with said gate spacers, exposing first surfaces of said layer of liner oxide where said liner oxide is interposed between said layer~~

~~of gate material and said gate spacers and where said liner oxide is furthest removed from the surface of said substrate, further exposing a second surface of said layer of liner oxide where said layer of liner oxide overlies the surface of said substrate;~~

~~applying~~ nitridizing~~nitridation to~~ said ~~first and second~~ exposed surfaces of said ~~layer of~~ liner oxides~~oxide~~, so as to form ~~creating~~ a layer of silicon oxy-nitride overlying ~~exposed surfaces of said gate electrode structure and~~ said exposed ~~first and second~~ surfaces of said ~~layer of~~ liner oxides~~oxide~~;

removing said liner oxides not covered by said gate spacers and said layer of silicon oxy-nitride; and

saliciding contact points to said gate electrode.

13 (Currently Amended): The method of claim 12, said applying nitridation to said first and second surfaces of said layer of liner oxide comprising a N_2[[/]] and H_2 plasma exposure.

14 (cancelled)

15. (original): The method of claim 12, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

16. (original): The method of claim 12, said layer of gate material comprising polysilicon.

17. (original): The method of claim 12, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

18. (original): The method of claim 12, said gate spacer material comprising silicon nitride.

19. (original): The method of claim 12, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

20. (original): The method of claim 12, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

21 (currently amended): The method of claim [[1]] 12, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.

22 (currently amended): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, ~~active surface regions having been defined in the surface of the substrate~~liner oxides with exposed surfaces formed over said substrate and on sidewalls of said gate electrode, gate spacers formed on said liner oxides;

~~creating a layer of gate oxide over the surface of the substrate;~~

~~depositing a layer of gate material over the surface of the substrate;~~

~~patterning and etching the layer of gate material and the layer of gate oxide, creating a gate electrode structure;~~

~~creating a layer of liner oxide over the surface of said substrate, including sidewalls and the surface of said gate electrode;~~

~~depositing a layer of gate spacer material over the surface of said layer of liner oxide;~~

~~etching said layer of gate spacer material, creating gate spacers over sidewalls of said gate electrode, thereby removing said layer of liner oxide from the surface of from sidewalls of said gate electrode where said layer of liner oxide is not covered with said gate spacers, exposing first surfaces of said layer of liner oxide where said liner oxide is interposed between said layer of gate material and said gate spacers and where said liner oxide is furthest removed from the~~

~~surface of said substrate, further exposing a second surface of said layer of liner oxide where said layer of liner oxide overlies the surface of said substrate;~~

nitridizing ~~the~~ said ~~first and second~~ exposed surfaces ~~surfaces~~ of said ~~layer of~~ liner oxides~~oxide, and second surfaces of said layer of liner oxide by exposing said first and second surfaces to a N_2/H_2 plasma at a temperature of about 250 degrees C.,~~ so as to form~~creating~~ a layer of silicon oxy-nitride overlying ~~exposed surfaces of said gate electrode structure and~~ said exposed ~~first and second~~ surfaces ~~surfaces~~ of said ~~layer of~~ liner oxides~~oxide~~;

removing said liner oxides not covered by said gate spacers and said layer of silicon oxy-nitride substantially without forming undercuts under said gate spacers; and

saliciding contact points to said gate electrode.

23. (original): The method of claim 22, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

24. (original): The method of claim 22, said layer of gate material comprising polysilicon.

25. (original): The method of claim 22, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

26. (original): The method of claim 22, said gate spacer material comprising silicon nitride.

27. (original): The method of claim 22, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

28. (original): The method of claim 22, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

29. (original): The method of claim 22, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.

30 (new): The method of claim 22, nitridizing said first and second surfaces of said layer of liner oxide comprising a N_2 and H_2 plasma exposure.

31 (new): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, liner oxides with exposed surfaces formed over said substrate and on sidewalls of said gate electrode, gate spacers formed on said liner oxides;

nitridizing said exposed surfaces of said liner oxides so as to form a layer of silicon oxy-nitride overlying an exposed surface of said gate electrode structure and said exposed surfaces of said liner oxides;

removing said liner oxides not covered by said gate spacers and said layer of silicon oxy-nitride substantially without forming divots on the liner oxides; and

saliciding contact points to said gate electrode.

32 (new): The method of claim 31, said applying nitridation to said first and second surfaces of said layer of liner oxide comprising a N_2 and H_2 plasma exposure.

33 (new): The method of claim 31, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

34 (new): The method of claim 31, said layer of gate material comprising polysilicon.

35 (new): The method of claim 31, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

36 (new): The method of claim 31, said gate spacer material comprising silicon nitride.

37 (new): The method of claim 31, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

38 (new): The method of claim 31, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

39 (new): The method of claim 31, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.

40 (new): The method of claim 31, wherein a difference of said heights of said gate spacers and said gate electrodes is about 600 Angstroms.